

FIG. 1

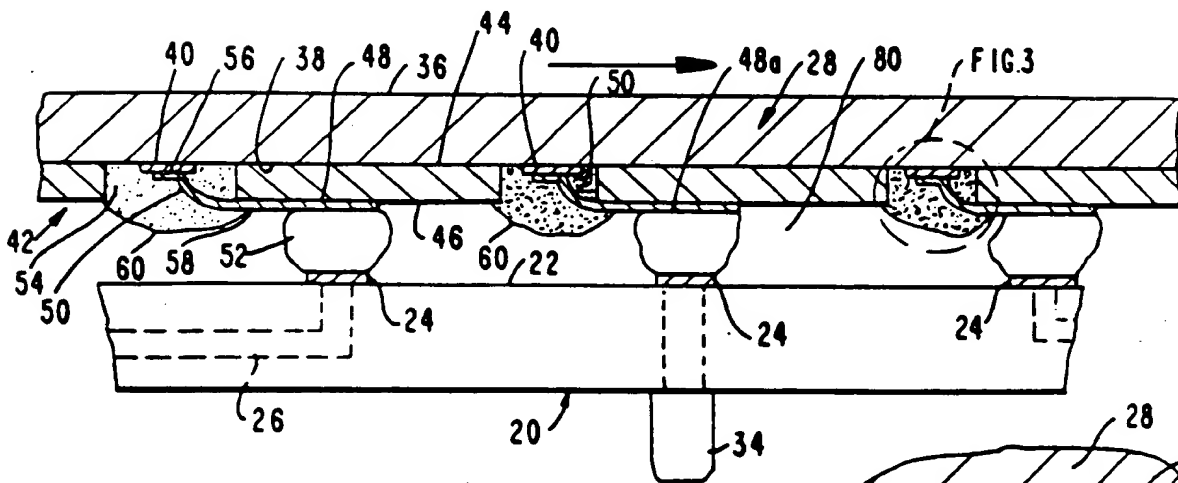


FIG. 2

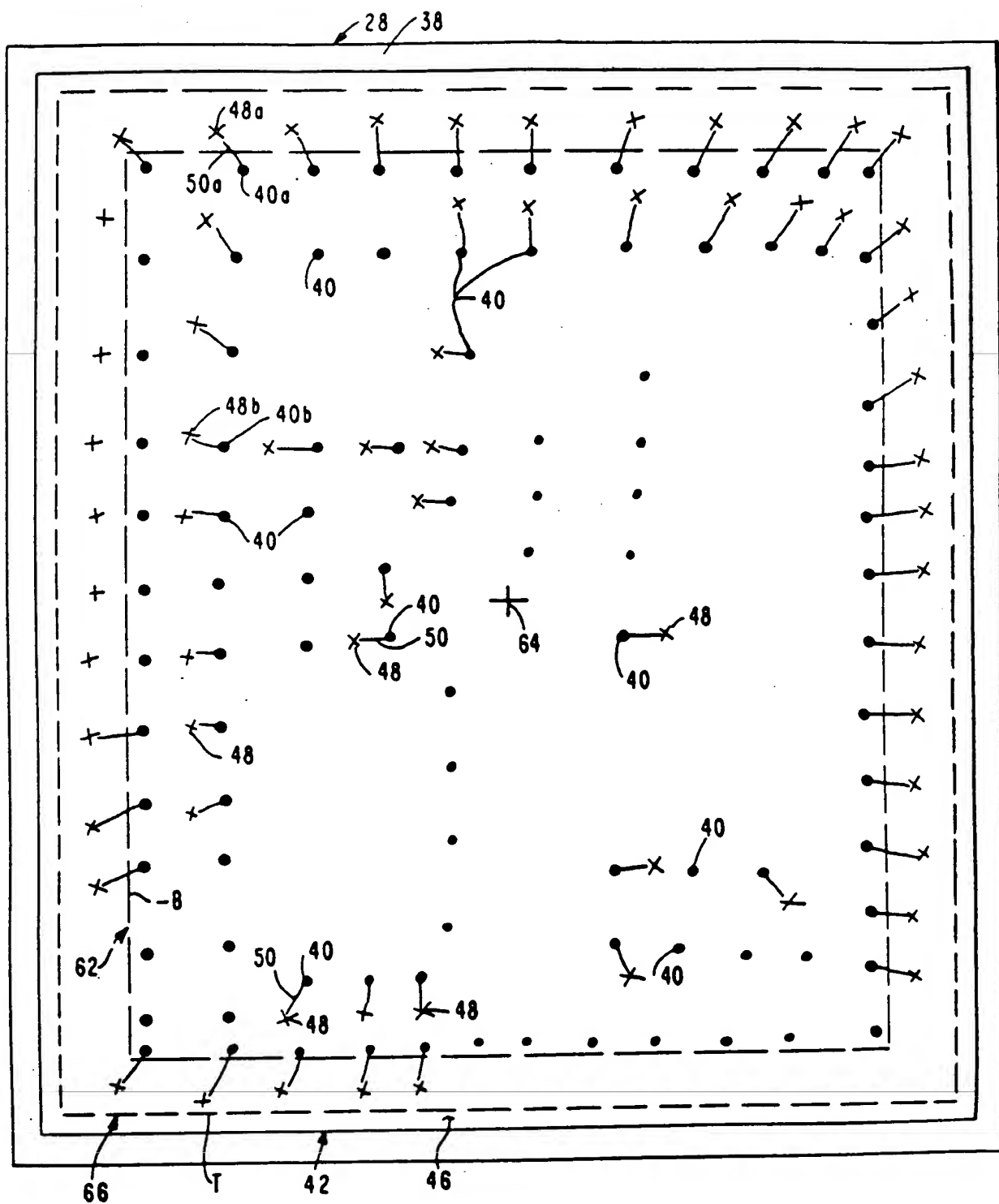


FIG. 4

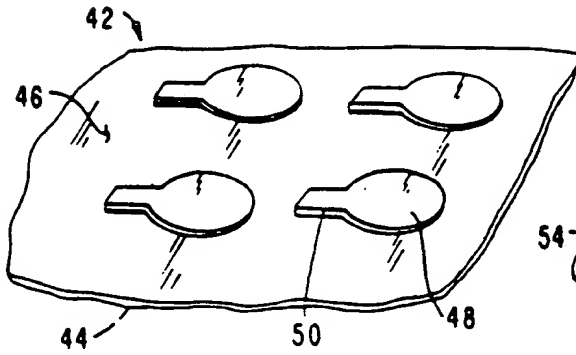


FIG. 5A

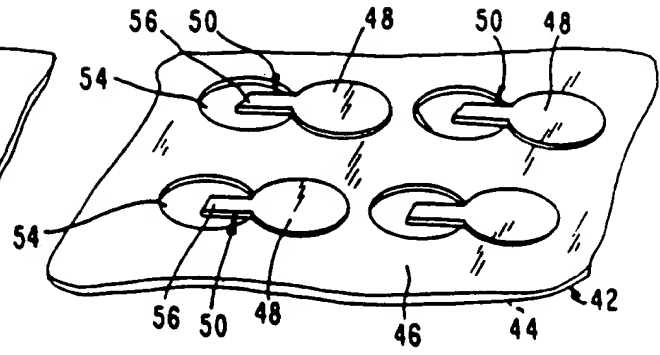


FIG. 5B

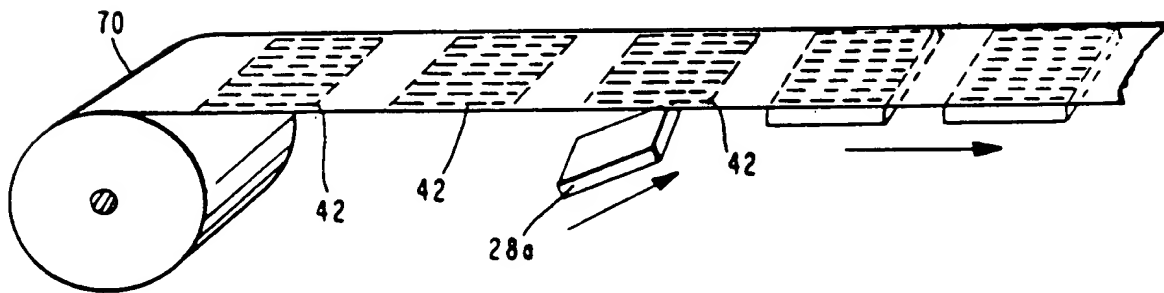


FIG. 6

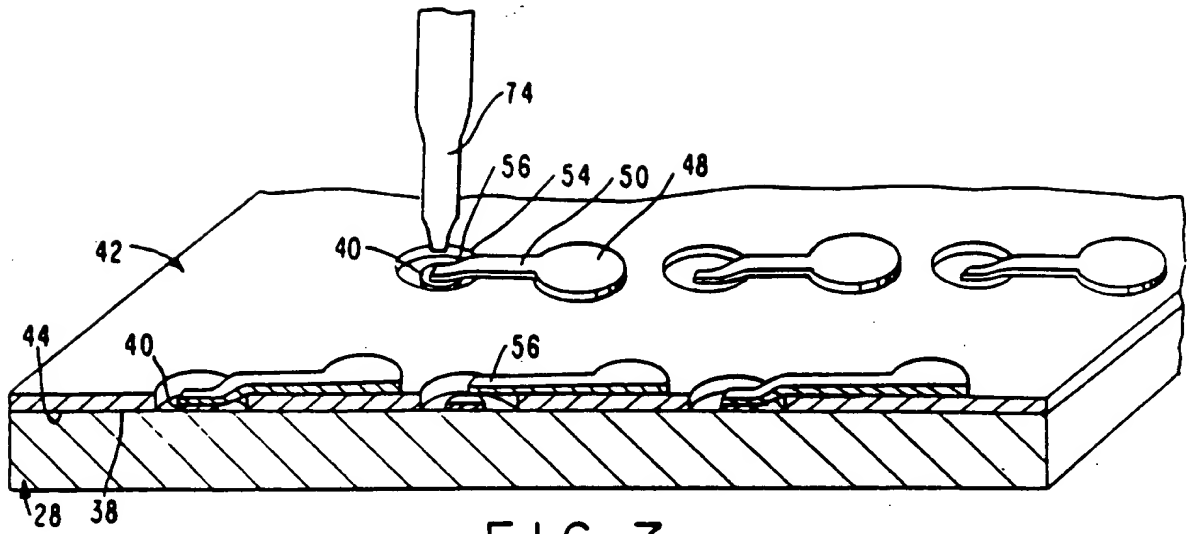


FIG. 7

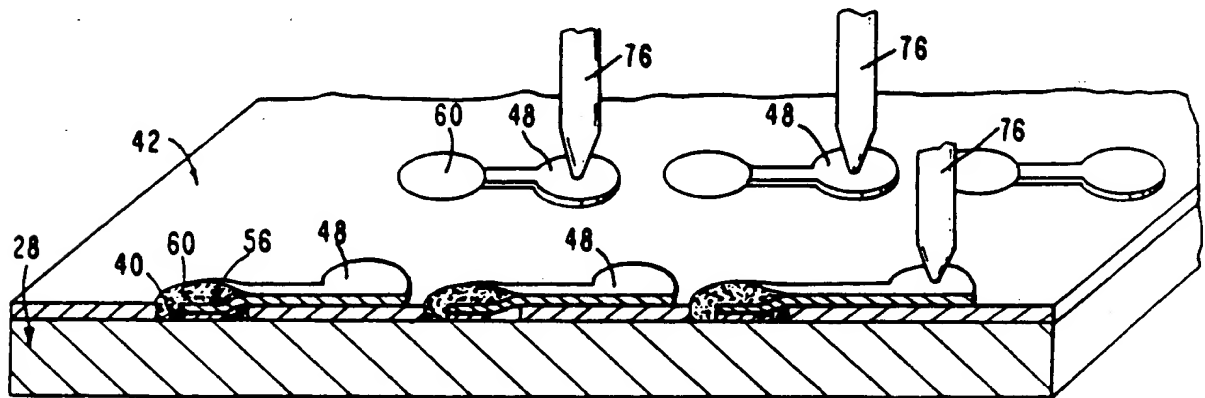


FIG. 8

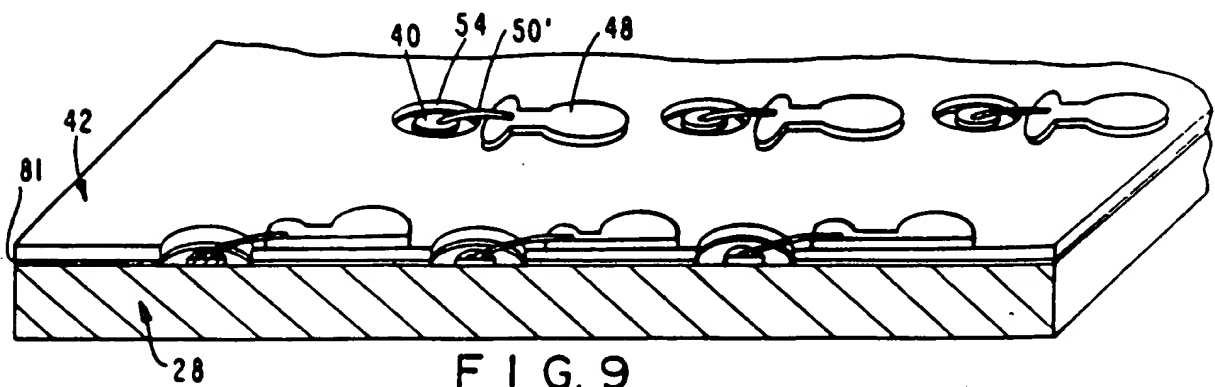


FIG. 9

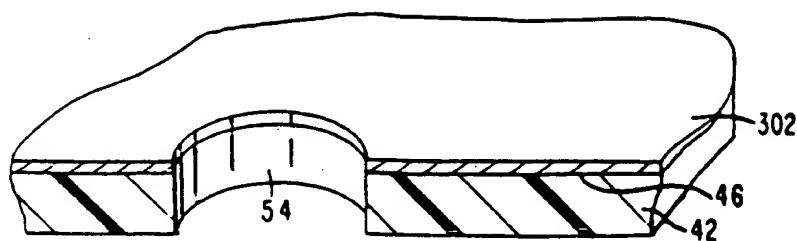


FIG. 10A

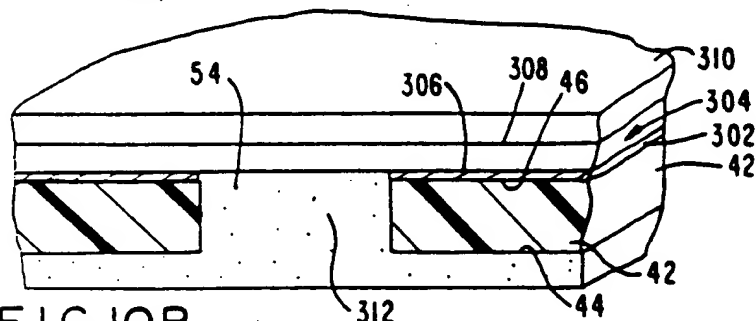


FIG. 10B

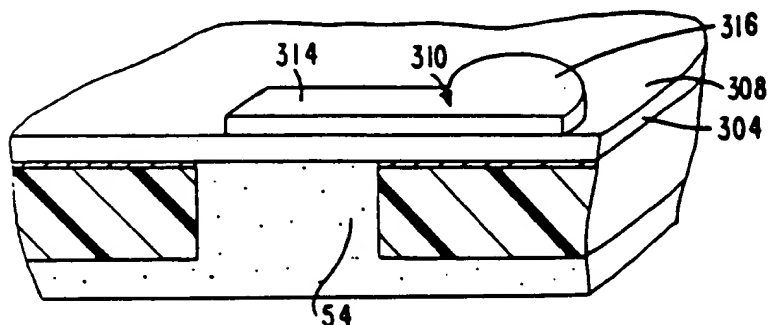


FIG. 10C

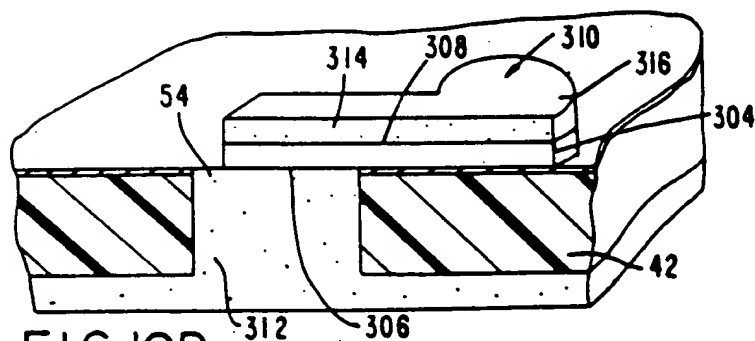


FIG. 10D

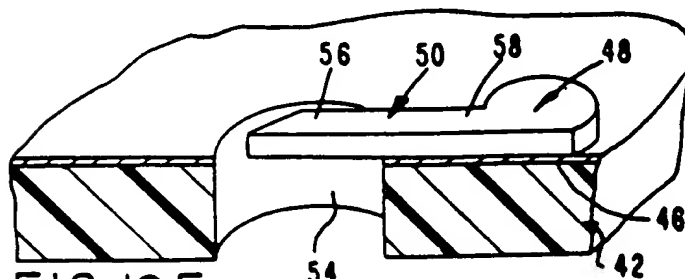


FIG. 10E

FIG. 11

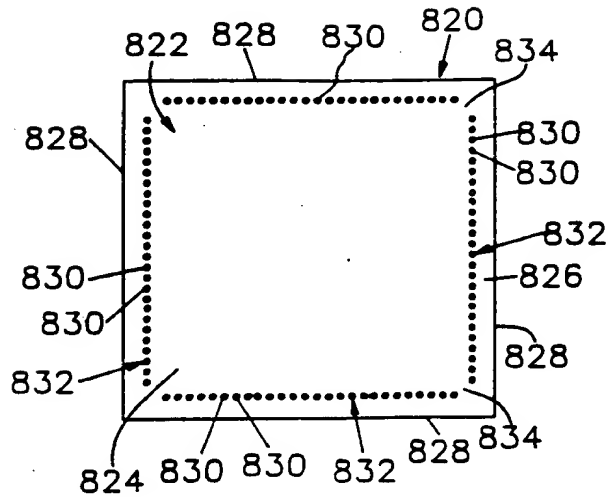


FIG. 12

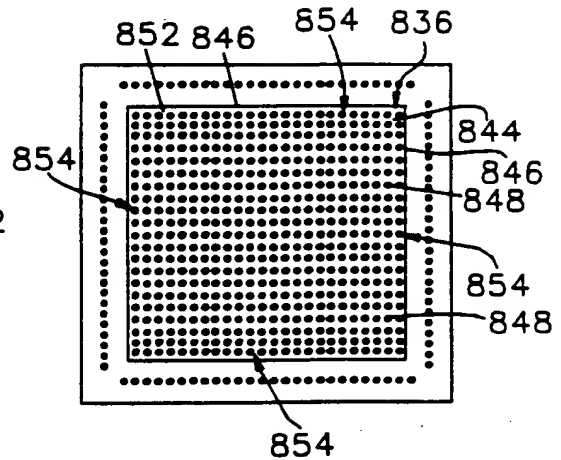


FIG. 17

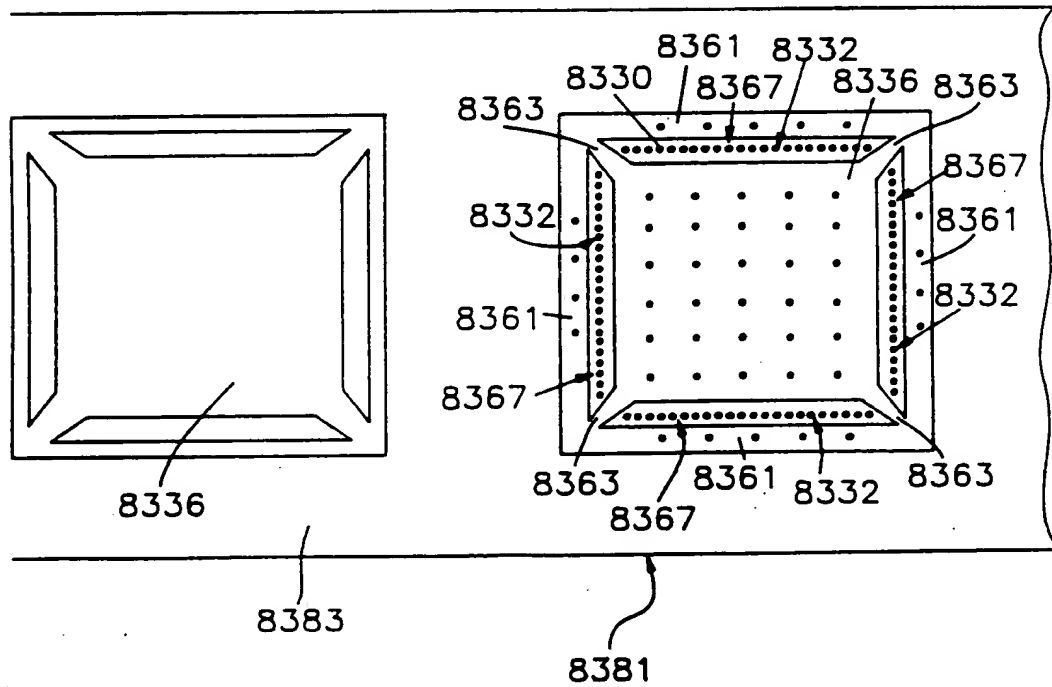


FIG. 13

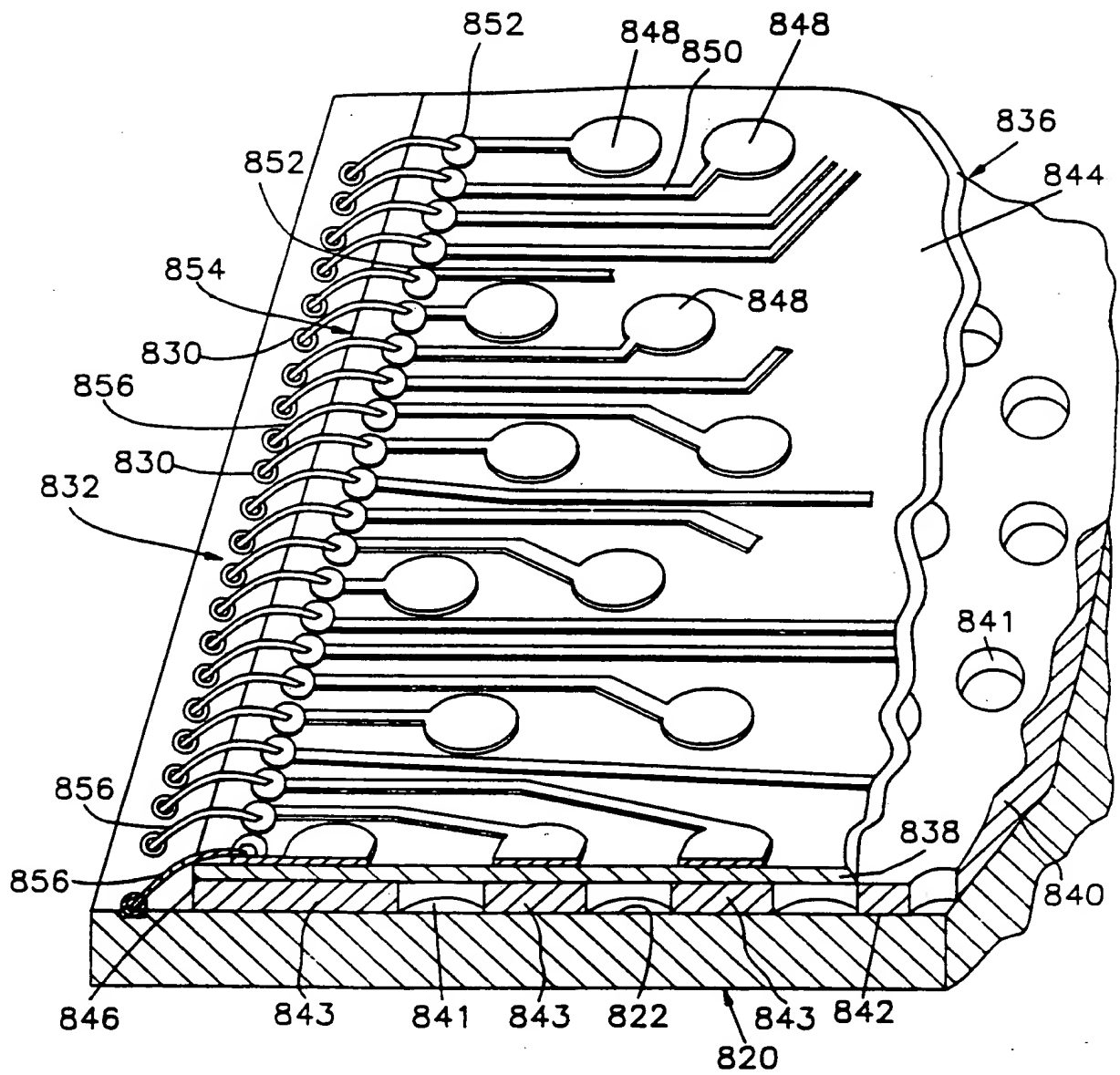


FIG. 14

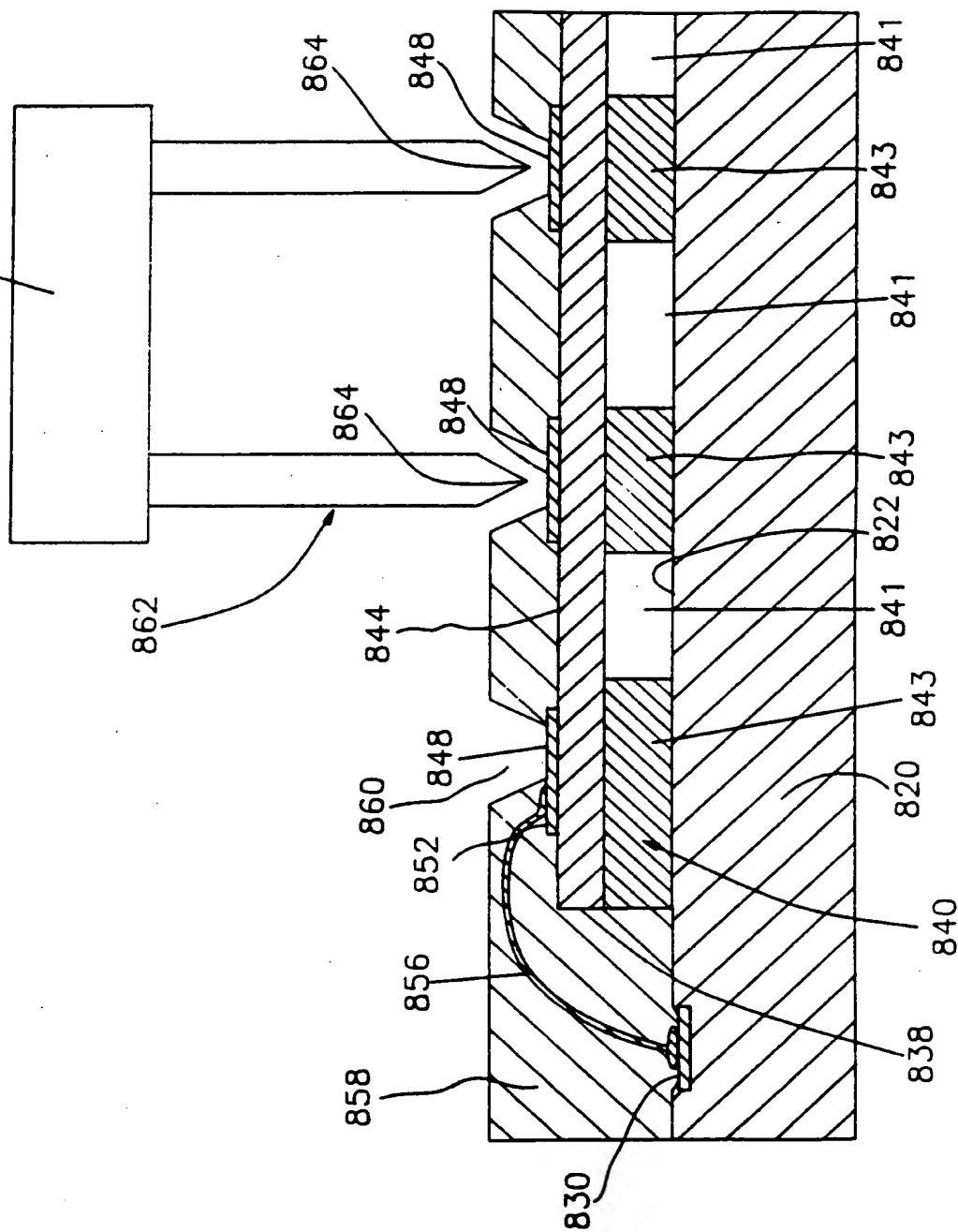
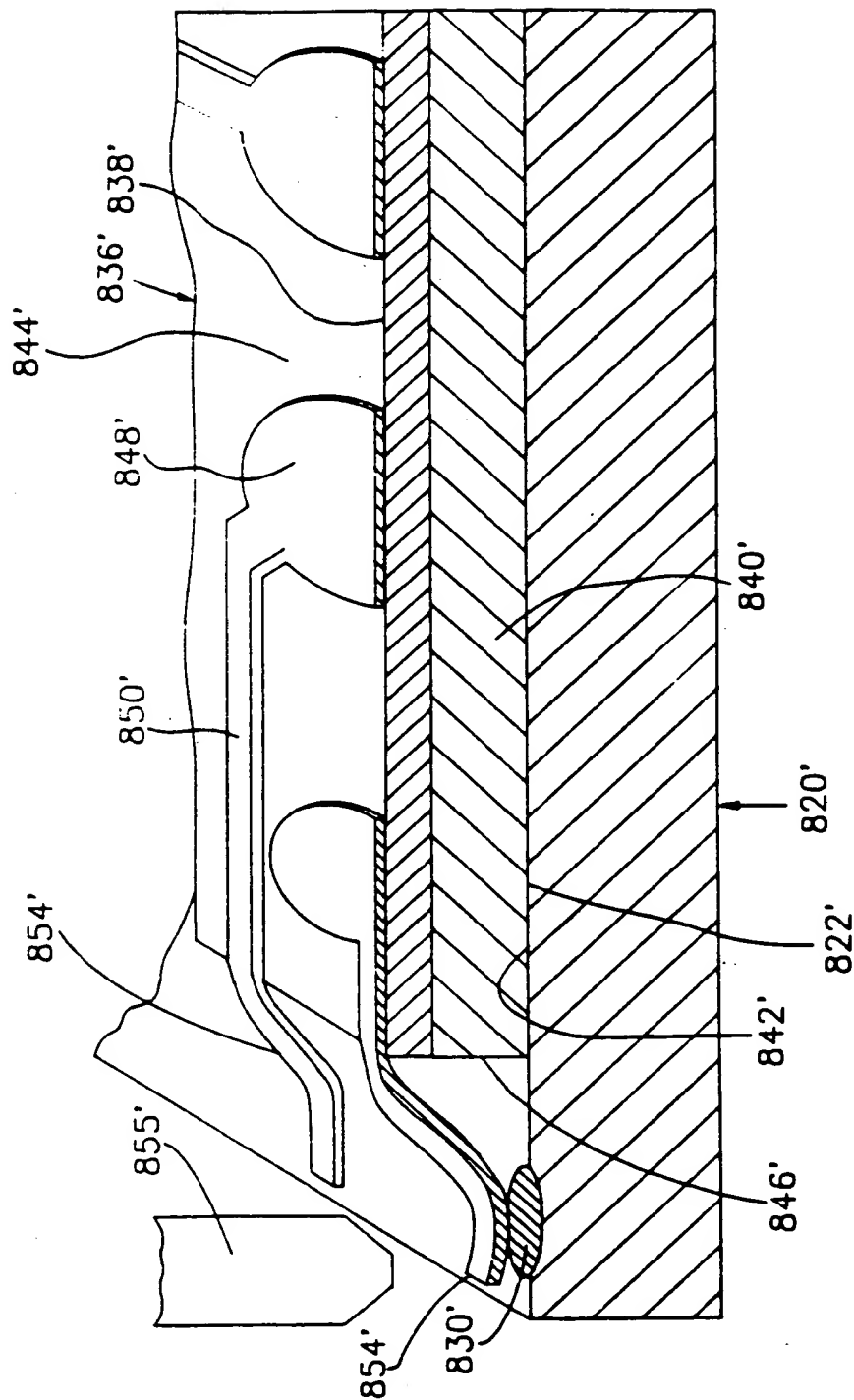


FIG. 15



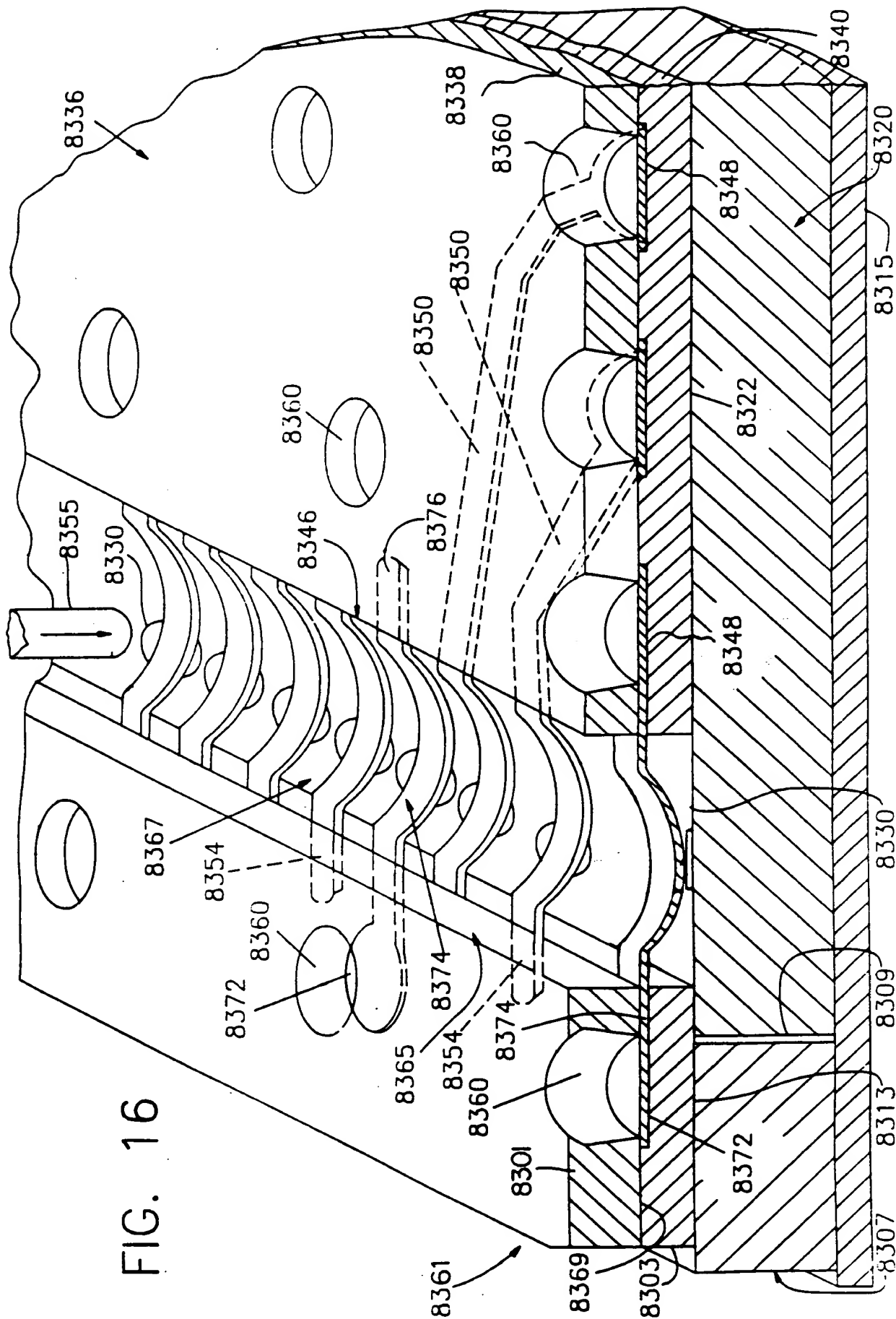


FIG. 18

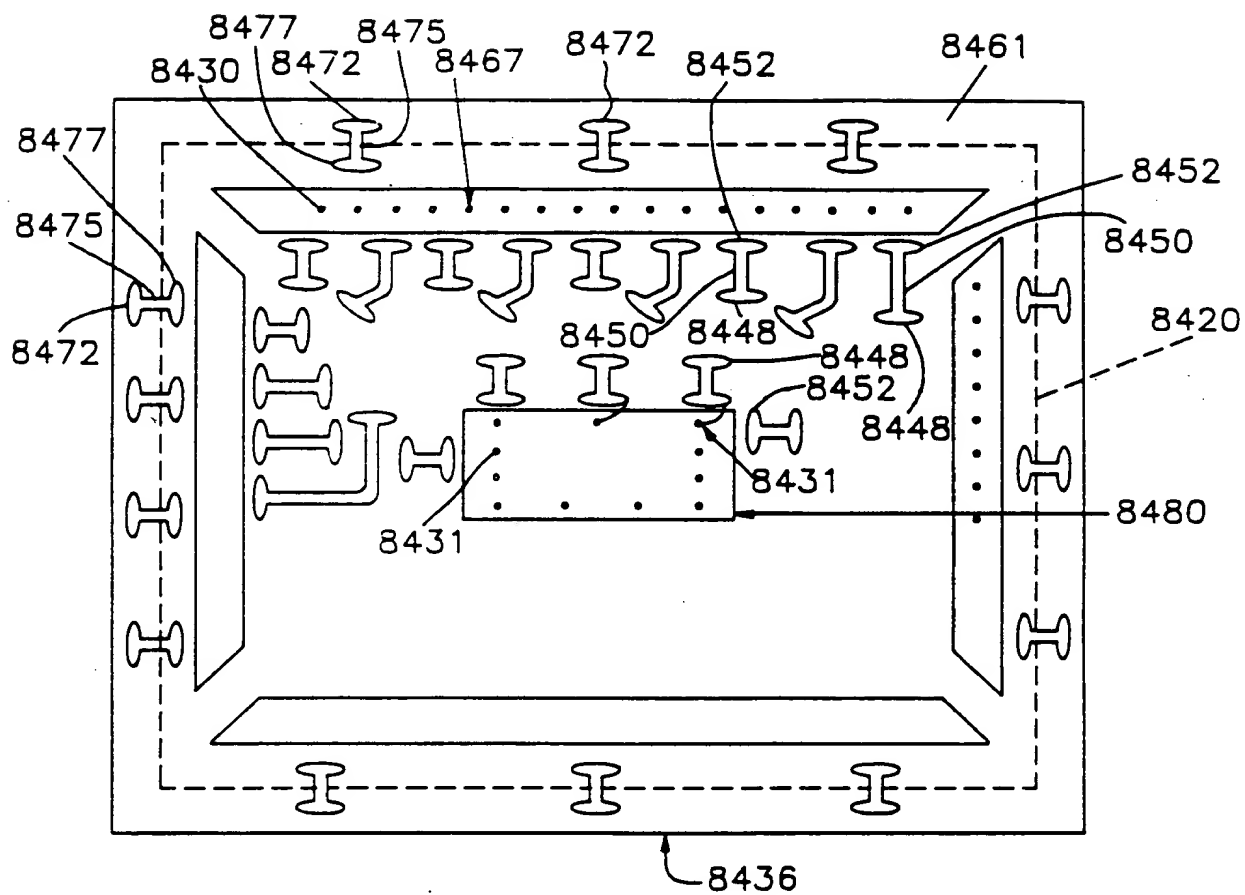
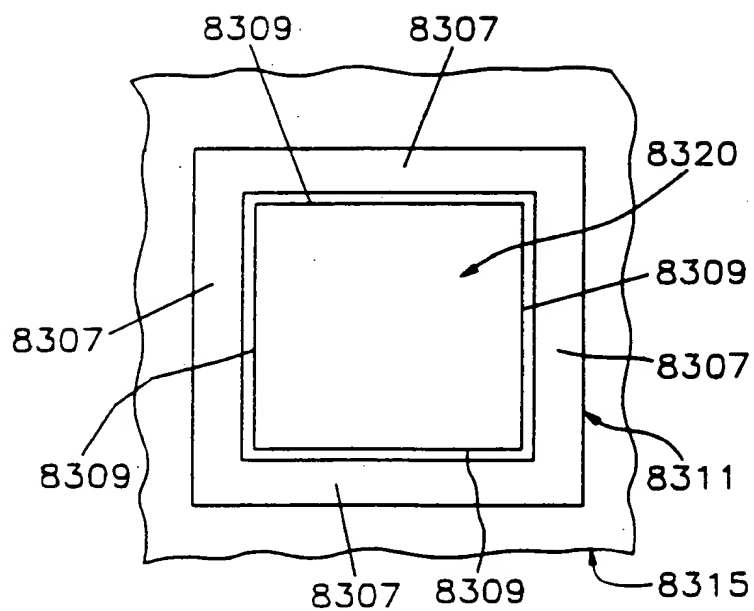


FIG. 19



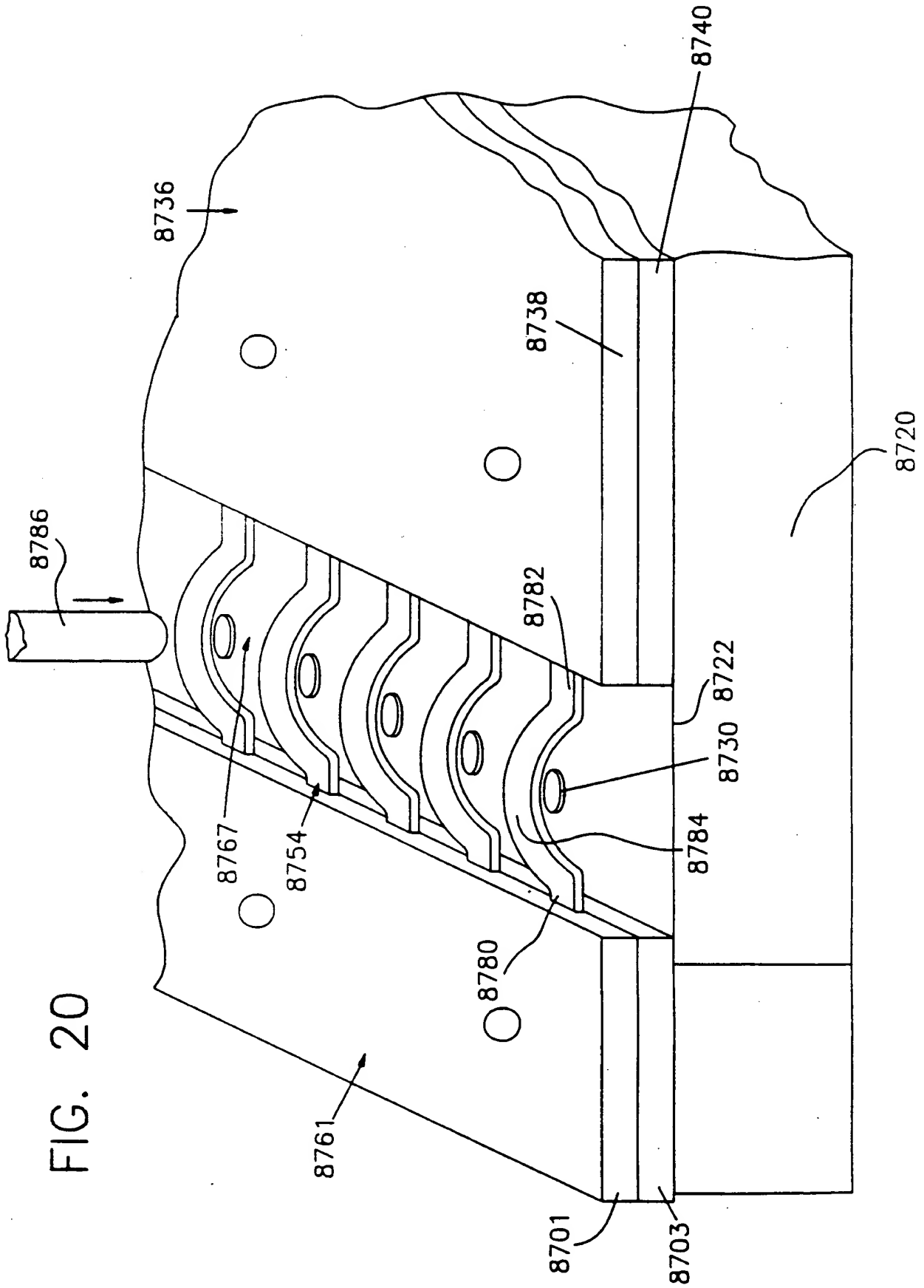


FIG. 21

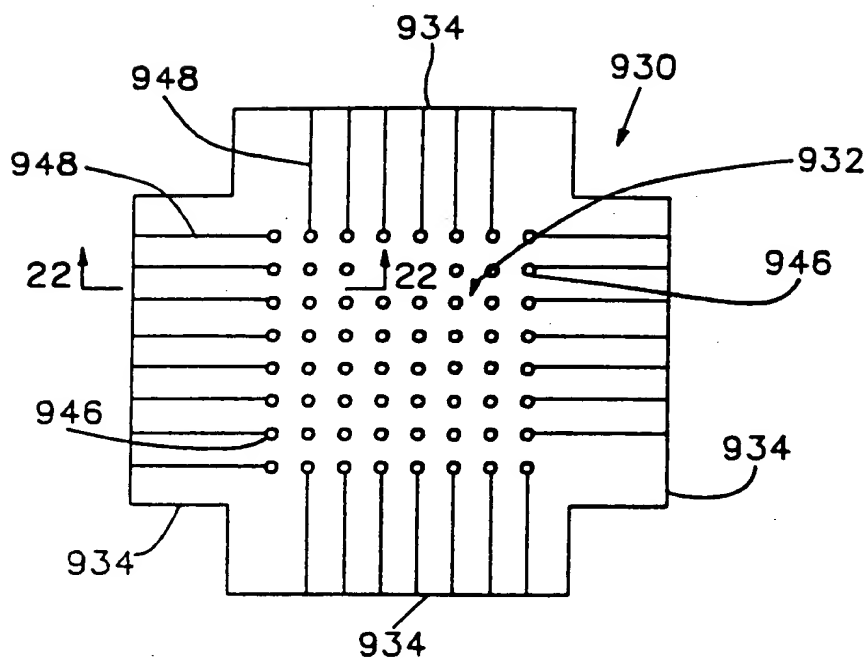
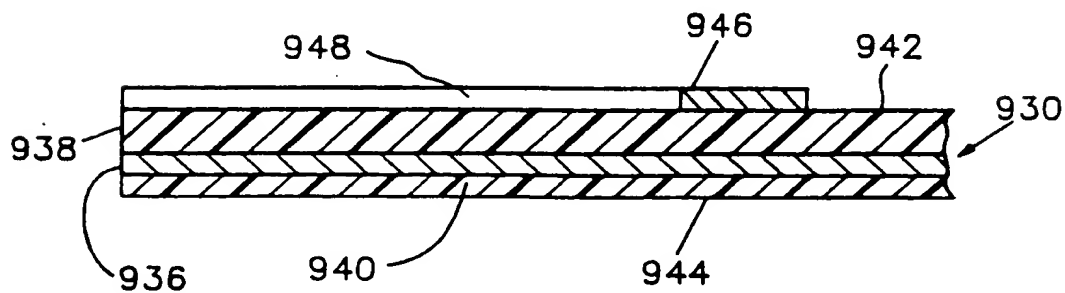


FIG. 22



A cross-sectional view of a device assembly 950. The assembly includes a substrate 952 with a top surface 954 and a bottom surface 958. A layer 956 is disposed on the top surface 954. A layer 960 is disposed on the bottom surface 958. A layer 962 is disposed between the layer 956 and the layer 960.

FIG. 25

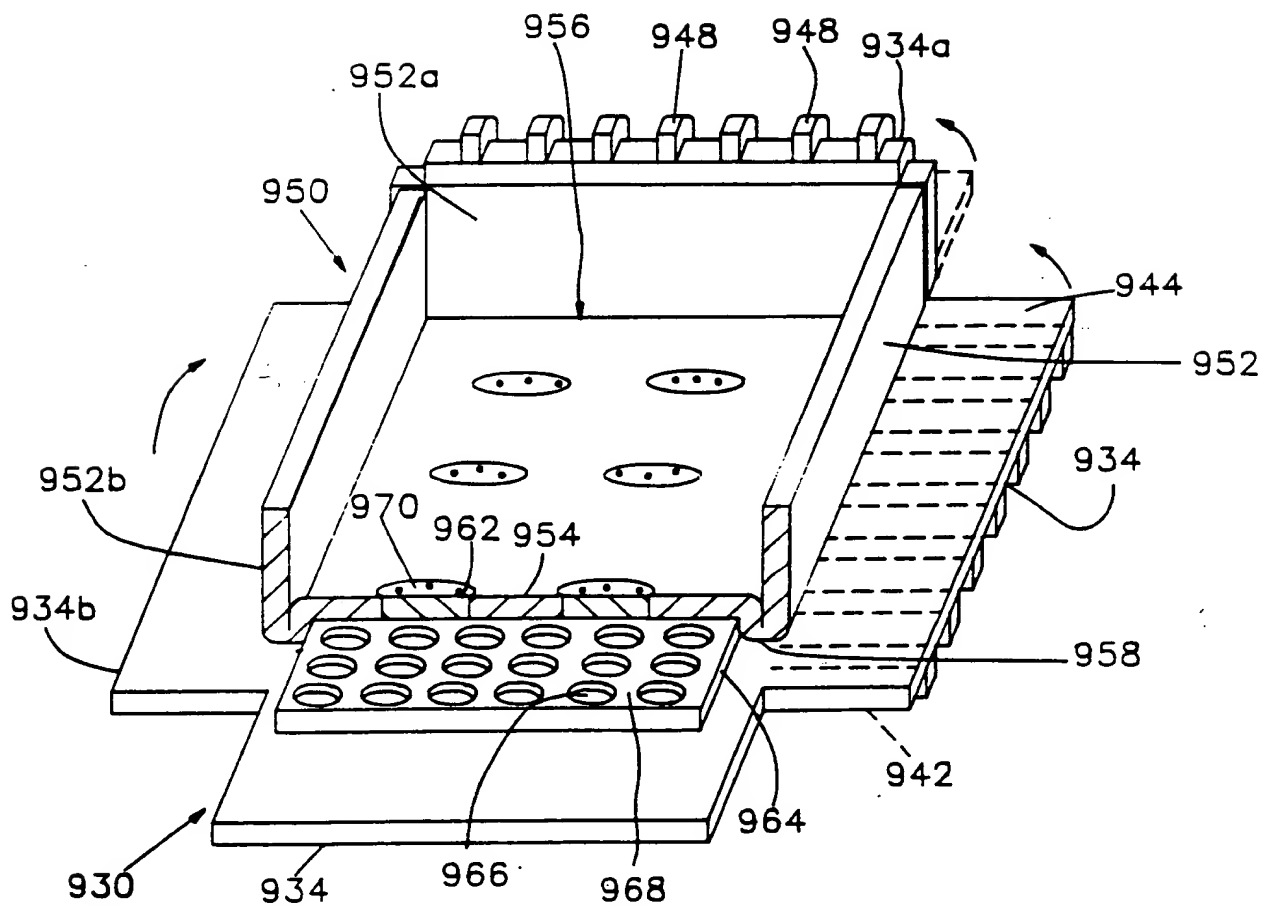
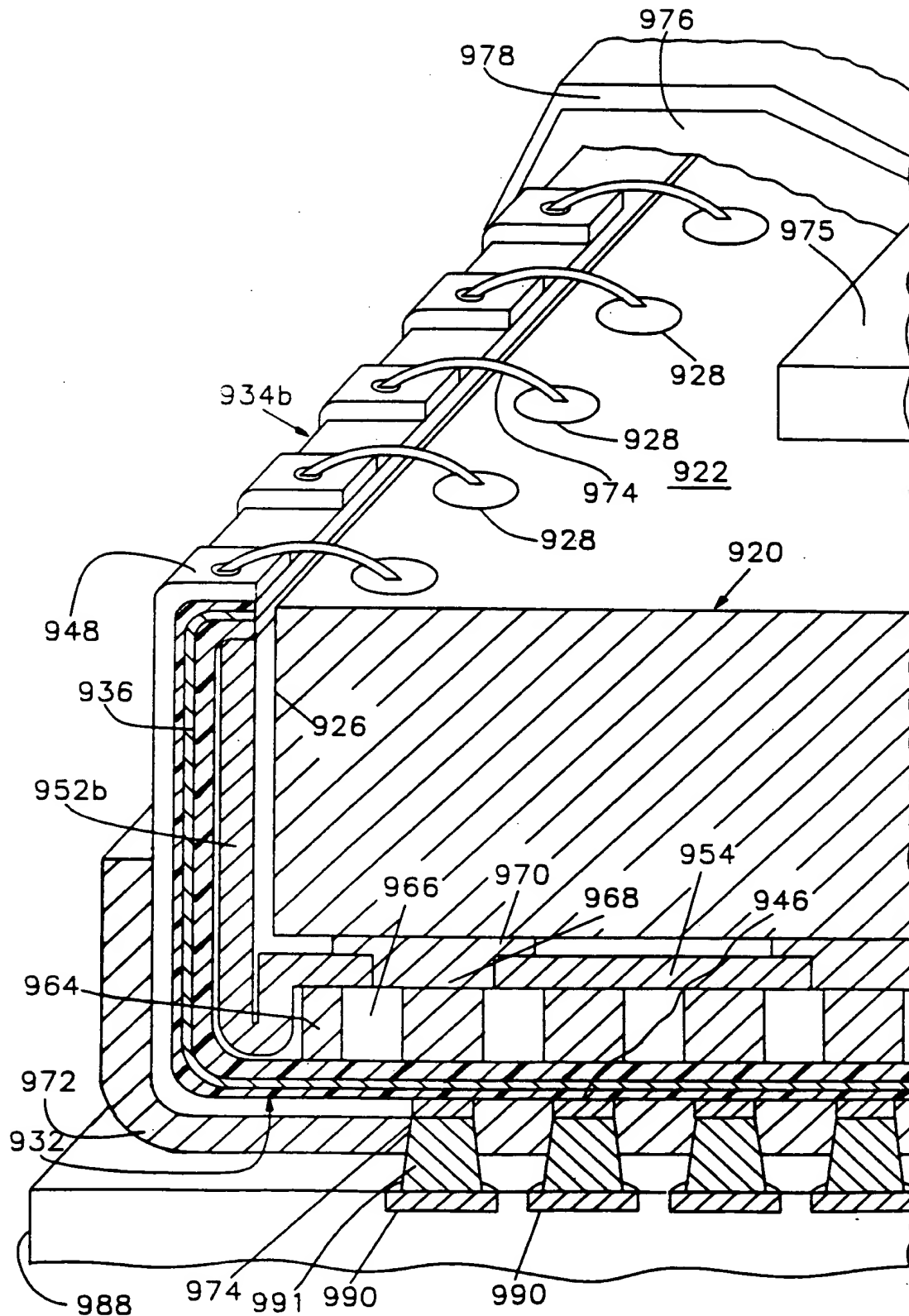


FIG. 26



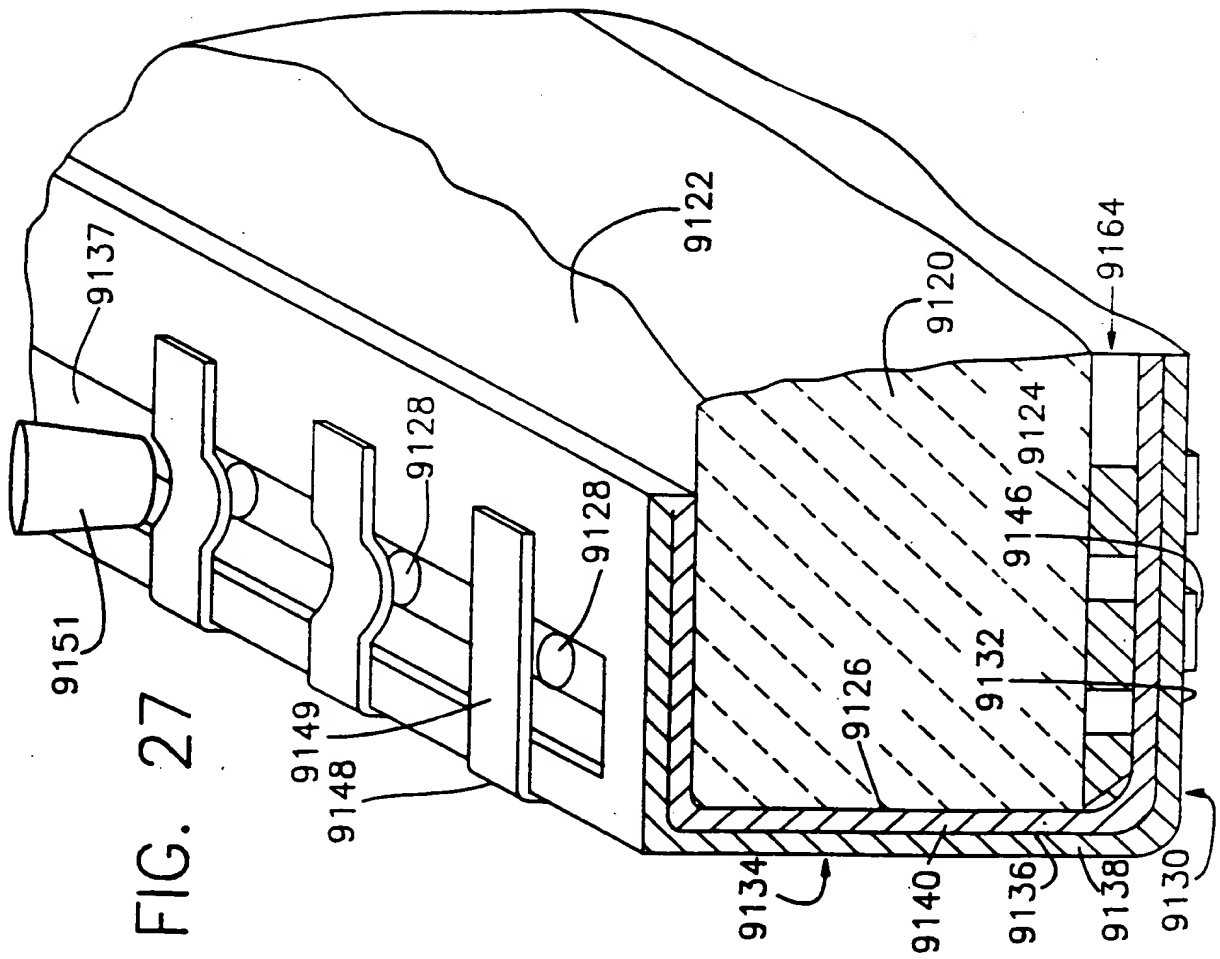


FIG. 28

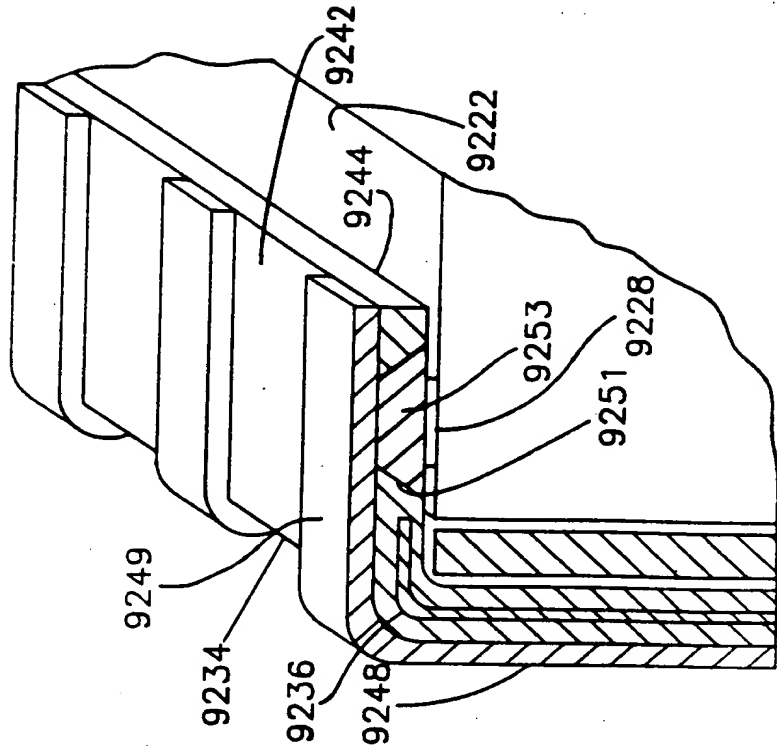


FIG. 29

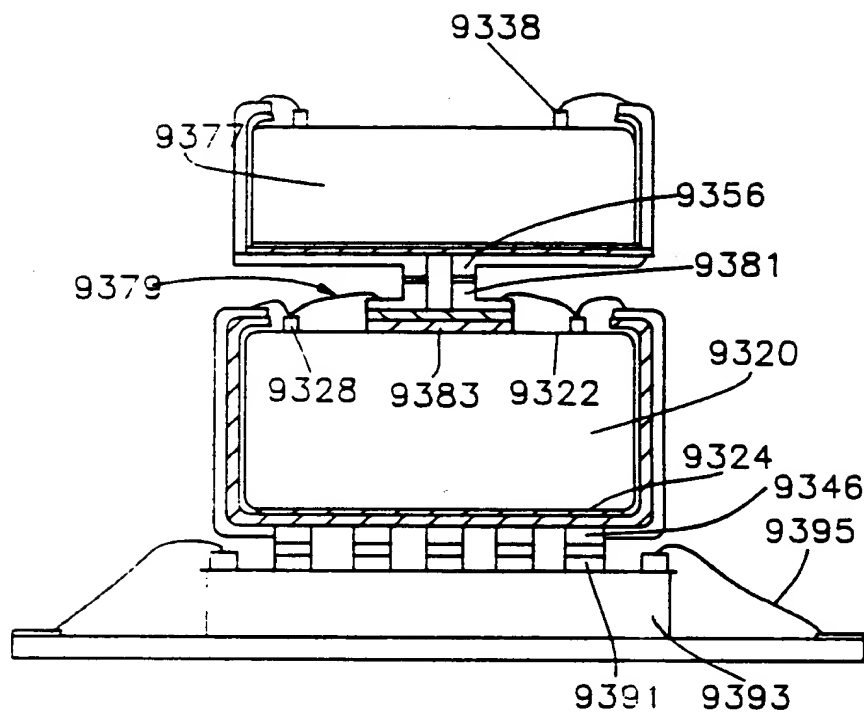


FIG. 30

